## AMENDMENTS TO THE CLAIMS

**Claims pending**

- At time of the Action: Claims 1-32.
- After this Response: Claims 1, 3-9, 12, 16-21, 23, 25, 26 and 29-47.

**Canceled or Withdrawn claims**: 2, 10, 11, 13-15, 22, 24, 27 and 28.

**Amended claims**: 1, 3, 8, 12, 17-21, 23, 25 and 26.

**New claims**: 33-47.

1. (Currently Amended) A method comprising:

creating mappings from ~~a logical~~received addresses ~~space~~ to physical memory by a hardware interface disposed between a processor and a number of physical memory devices; and

~~identifying portions of the logical address space based on usage;~~

modifying the mappings by the hardware interface to reduce the number of physical memory devices that are targeted by the mappings~~; and~~

~~receiving memory instructions that reference memory in terms of the logical address space~~.

2. (Cancelled)

3. (Currently Amended) A memory controller comprising:

means for receiving memory instructions from a processor that specifies memory addresses ~~that reference memory~~ in terms of a logical address space;

means for identifying portions of the logical address space based on usage; and

means for mapping the identified portions of the logical address space to physical memory in a manner that reduces the number of physical memory devices referenced by the identified portions of the logical address space .

4. (Original) A memory controller as recited in claim 3, wherein the means for identifying include means for monitoring the memory instructions to determine more frequently used portions of the logical address space.

5. (Original) A memory controller as recited in claim 3, wherein the means for identifying include means for monitoring the memory instructions to determine more recently used portions of the logical address space.

6. (Original) A memory controller as recited in claim 3, wherein the means for identifying include means for receiving notifications regarding logical memory allocations and de-allocations.

7. (Original) A memory controller as recited in claim 3, wherein the means for identifying include means for receiving notifications regarding actual usage of logical memory addresses.

8. (Currently Amended) A memory controller as recited in claim 3, wherein the means for identifying action include means for maintaining one or more in-use registers indicating whether corresponding portions of physical memory are currently in use.

9. (Original) A memory controller as recited in claim 3, further comprising:

means for identifying one or more memory devices that are not referenced by the identified portions of the logical address space; and

means for setting said one or more identified memory devices to a reduced power mode.

10-11. (Canceled)

12. (Currently Amended) A memory controller as recited in claim 3, further comprising:

means for identifying one or more physical memory areas that are relatively infrequently referenced by the identified portions of the logical address space; and

means for setting said one or more physical memory areas to a reduced power mode.

13-15. (Canceled).

16. (Original) A memory controller as recited in claim 3, further comprising:

a means for periodically repeating the identifying and mapping actions to repeatedly reduce the number of physical memory devices referenced by the identified portions of the logical address space; and

means for moving affected portions of physical memory so that each logical address continues to reference the same data prior to any repeated mapping action.

17. (Currently Amended) A method of managing memory, comprising:

monitoring memory accesses received from a processor to identify portions of ~~a logical~~the processor's address space based on usage; and

periodically re-mapping the ~~logical~~ processor's address space to physical memory to reduce the number of physical memory devices referenced by the identified portions of the ~~logical~~ processor's address space.

18. (Currently Amended) A method as recited in claim 17, wherein the monitoring comprises monitoring the memory instructions to determine more frequently used portions of the ~~logical~~ processor's address space.

19. (Currently Amended) A method as recited in claim 17, further wherein the monitoring comprises monitoring the memory instructions to determine more recently used portions of the ~~logical~~ processor's address space.

20. (Currently Amended) A method as recited in claim 17, further comprising:

receiving memory instructions that reference memory in terms of the ~~logical~~ processor's address space; and

monitoring the memory instructions to identify the portions of the ~~logical~~ processors address space..

21. (Currently Amended) A method as recited in claim 17, wherein the identified portions of the ~~logical~~ processor's address space are those portions that are used least frequently, further comprising:

identifying one or more memory devices that are not referenced by the identified portions of the ~~logical~~ processor's address space; and

setting said one or more identified memory devices to a reduced power mode.

22. (Canceled).

23. (Currently Amended) A method as recited in claim 17, wherein the identified portions of the ~~logical~~ processor's address space are those portions that are used least frequently, further comprising:

identifying one or more physical memory areas that are not referenced by the identified portions of the ~~logical~~ processor's address space; and

setting said one or more physical memory areas to a reduced power mode.

24. (Canceled).

25. (Currently Amended) A method as recited in claim 17, further comprising:

prior to any re-mapping action, moving affected portion of physical memory so that ~~each logical~~ addresses received from the processor continues ~~to~~ reference the same data.

26. (Currently Amended) A system comprising:

~~a plurality of physical memory devices containing physical memory;~~

~~a memory controller configured to reference the physical memory in response to received memory instructions specifying addresses in terms of a logical address space;~~

an operating system configured to dynamically allocate memory from ~~the~~ a logical address space and to identify allocated portions of the logical address space to ~~the~~ a memory controller;

the operating system further configured to dynamically de-allocate memory from the logical address space and to identify the de-allocated portions of the logical address space to the memory controller;

wherein the memory controller is configured to ~~respond to the operating system by mapping~~ map allocated portions of the logical address space to corresponding portions of physical address space ~~memory~~ in a manner that tends to reduce the number of physical memory devices referenced by the allocated portions of the logical address space; and

the memory controller further configured to move portions of memory regions corresponding to allocated portions of the logical address space in response to identification of de-allocated portions of the logical address space and re-mapping the corresponding portions of the physical address space and

corresponding portion of the logical address space to reduce the number of physical memory devices referenced by allocated portion of logical memory.

27-28. (Canceled).

29. (Original) A memory management system comprising:

means for maintaining a free region list indicating free memory regions for potential allocation from physical memory devices;

means for sorting the free region list in an order that is based on the relative current allocations of memory regions from respective sets of one or more physical memory devices; and

means for allocating memory regions indicated by the sorted free region list on the sorted order so that the memory regions are allocated preferentially from those physical memory devices having higher relative current allocations of memory regions.

30. (Original) A memory management system as recited in claim 29, further comprising:

means for identifying one or more memory devices having relatively lower current allocations of memory regions; and

means for setting said one or more identified physical memory devices to a reduced power mode.

31. (Original) A memory management system as recited in claim 29, further comprising means for maintaining the free region list as a linked list of free region indicators.

32. (Original) A memory management system as recited in claim 29, further comprising means for repeatedly re-sorting the free region list in said order.

33. (New) The system as recited in Claim 26, further comprising:

identifying one or more of a plurality of memory devices having relatively lower allocated portions of memory regions; and

setting the identified one or more of the plurality of memory devices to a reduced power state.

34. (New) The system as recited in Claim 26, further comprising:

identifying one or more of the plurality of memory devices based on relatively lower usage; and

setting the identified one or more of the plurality of memory devices to a reduced power state.

35. (New) The system as recited in Claim 34, wherein identifying one or more of the plurality of memory device based on relatively lower usage comprises monitoring memory instructions to determine relatively less frequently used portions of the physical address space.

36. (New) The system as recited in Claim 34, wherein identifying one or more of the plurality of memory device based on relatively lower usage comprises monitoring memory instructions to determine relatively least recently used portions of the physical address space.

37. (New) The memory controller as recited in claim 3, wherein the means for identifying include means for identifying portions of the processor's physical address space based on frequency of usage.

38. (New) The memory controller as recited in claim 3, wherein the means for identifying include means for identifying portions of the processor's physical address space based on most recent usage.

39. (New) The method as recited in Claim 1, further comprising receiving memory instructions from a processor or graphics adapter by the hardware interface.

40. (New) The method as recited in Claim 1, wherein the mappings are modified at the hardware interface independently of the operating system.

41. (New) The method as recited in Claim 1, further comprising refreshing the content of physical memory devices by the hardware interface independently of the operation system

42. (New) The method as recited in Claim 1, further comprising:

identifying one or more of the plurality of memory devices referenced by relatively few mappings; and

setting the identified one or more of the plurality of memory devices to a reduced power state.

43. (New) The method as recited in Claim 1, wherein the received addresses are specified by a processor in terms of a physical address space, further comprising:

identifying portions of the processor's physical address space based on usage;

re-mapping the identified portions of the processor's physical address space to physical memory by the hardware interface in a manner that reduces the number of physical memory devices referenced by the identified portions of the processor's physical address space; and

prior to re-mapping, moving the corresponding memory content so that the corresponding memory content will continue to be referenced by the same received address.

44. (New) The method as recited in Claim 43, wherein the re-mapping is periodically performed after a pre-defined number of memory references.

45. (New) The method as recited in Claim 43, wherein the re-mapping is performed after power consumption by the physical memory reaches a determined threshold.

46. (New) The method as recited in Claim 43, wherein the re-mapping is periodically performed after a pre-defined number of memory allocations.

47. (New) The method as recited in Claim 43, wherein the re-mapping is performed at periodic time intervals.